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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,506	09/30/2003	Eric J. Strang	231753US6YA	1663

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EF

Office Action Summary	Application No.	Applicant(s)	
	10/673,506	STRANG, ERIC J.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/673,506 filed on 9/30/2003. Claims 1-66 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-25, 32-56 and 63-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Sonderman et al. (6,802,045).

4. As to claims 1, 32, 63 and 66, Sonderman et al. teach substantially similar claimed invention of a method and apparatus for analyzing a process performed by a semiconductor processing tool (Fig. 1-8 and its description) comprising inputting data relating to a process performed by the semiconductor processing tool (process data, input data; at least col. 3 lines 50-64; Fig. 1); inputting a first principles physical model relating to the semiconductor tool (device physics model, at least in col. 5; Fig. 3); performing first principle simulation using the input data and the physical model to provide a first principles simulation results (Fig. 1-5; col. 5-7; simulation data result, simulation data); and using the first principles simulation result to determine a fault in the process performed by the semiconductor processing tool (Fig. 1-8, col. 5-7).

5. As to claims 2, 33 Sonderman et al. teach directly inputting the data (input data, process, manufacturing data, input control parameters) relating to a process performed by the semiconductor processing tool from at least on the physical sensor and a metrology tool physically mounted on the semiconductor processing tool (Fig. 1, 7, col. 4-8).

6. As to claims 3-5, 34-36, Sonderman et al. teach indirectly inputting the data relating to a process performed by the semiconductor processing tool from at least one of a manual input device and a database, inputting data recorded from a process previously performed by the semiconductor processing tool, inputting data set by a simulation operator (Fig. 1-3, col. 1, manual fashion and automated fashion, col.4-7).

7. As to claims 6-9, 37-40, Sonderman et al. teach inputting data relating to at least one of the physical characteristics of the semiconductor processing tool and the semiconductor tool environment, data relating to at least one of a characteristic and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model of the geometry (modified models) of the semiconductor processing tool; inputting fundamental equations necessary to perform first principles simulation for a desired simulation result (Fig. 1-3, col. 5-9).

8. As to claims 10-13, 41-44, Sonderman et al. performing interaction concurrently between simulation environment (first principles simulation) and the semiconductor processing tool (Fig. 2); performing simulation environment (first principles simulation) and the semiconductor processing tool (Fig. 2); performing first principles simulation

using the input data to set a boundary condition and an initial condition of the first principles simulation model (Fig. 3, col. 5-8).

9. As to claims 14, 45, Sonderman et al. teach using the simulation result (simulation data, simulation data result) to detect a fault in the process performed by the semiconductor processing tool by comparing the first principles simulation result with the input data (col. 7, Fig. 5-7).

10. As to claims 15-19, 46-50,Sonderman et al. teach a system having a network of interconnected resources to perform at least one of the process steps as recited in Claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principles simulation; sharing simulation information among interconnected resources to determine the fault in the process performed by the simulation processing tool; distributing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principles simulations by different resources; distributing model changes among the interconnected resources to redundant refinements of first principles simulations by different resources (Fig. 1-3, computer code software is described in col. 9 starting line 58; col. 5-8).

11. As to claims 20-21, 51-52, Sonderman et al. teach remote access (Col. 9 line 58 to col. 10 line 31). Note that a wide area network is art inherent.

12. As to claims 22, 53, Sonderman et al. teach performing simulation utilizing a computer software code (Col. 9 line 58 to col. 10 line 31).

13. As to claims 23-25, 54-56, Sonderman et al. teach using the first principles simulation result (simulation data set results) to classify a fault in the process performed by the semiconductor processing tool (col. 6, lines 1-35); calculating a set of perturbations solutions corresponding to the first principles simulation for input data to generate a profile data solutions to the first principles simulation, inputting the perturbation solutions to a multivariate analysis; inputting a difference between the first principles simulation result and the input data to the multivariate analysis; and utilizing the multivariate analysis to identify a correlation between the input data and the difference (defining variations into the components of defined models in order to simulate the effects of online manufacturing performance by the models; modified models) (col. 5-8).

14. As to claims 64-65, Sonderman et al. teach interaction between simulation environment, process control environment and manufacturing/processing environment (sharing computational load of the simulation, sharing simulation information among interconnected resources) (Fig. 1-3).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 26-31 and 57-62 are rejected under 35 U.S.C. 103(a) as being obvious over Sonderman et al. (6,802,045) in view of Fatke et al. (US 2005/0016947).

17. As to claims 26-28, 57-59, Sonderman et al. do not explicitly teach the multivariate analysis comprising a partial least square analysis; defining a set of loading coefficients, computing at least one of mean and standard deviation values. Fatke et al. teach these limitations including defining a correlation matrix in order to improve detection of a feature etch completion process during semiconductor manufacturing to thereby providing accurate and precise completion of an etch process (see abstract, Fig. 4, summary, 0051). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to combine these teachings in to the system as taught by Sonderman et al. in order to provide an accurate and precise completion of a process during semiconductor manufacturing.

18. As to claims 29-31, 60-62, Sonderman et al. attributing the difference between simulated results and input data to one input data using the correlation; using the simulation result to detect a fault comprising detecting a fault (error) in at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposit system, a rapid thermal processing system for thermal annealing and a batch diffusion furnace (examples described in col. 4; detecting a fault in at least one of a chemical vapor deposition system and a physical vapor deposition system (col. 4, 6, 7, 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER